## IN THE CLAIMS:

Please cancel claims 1-24, 29 and 30 without prejudice or disclaimer.

Please amend claim 25 as follows:

Butt D'

25. (Twice Amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having a first surface and a second surface;

at least one [first doped area] p-well and at least one n-well on said substrate first surface; [and]

at least one p-type area within said at least one n-well;

at least one n-type area within said at least one p-welk and

a substantially dopant-free, uninterrupted diffusion barrier layer over said at least one <u>p-well and</u> said at least one <u>n-well</u> [first doped area] on said substrate first surface.

Please add the following new claims:

Subt D2

33. A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having a first surface and a second surface;

at least one p-well and at least one n-well on said substrate first surface;

at least one doped area within at least one of said at least one n-well and said at least one p-well;

a substantially dopant-free, uninterrupted diffusion barrier layer over said at least one p-well and said at least one n-well on said substrate first surface.

34. The structure of claim 33 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.



- 35. The structure of claim 33 wherein said substantially dopant-free, uninterrupted diffusion barrier layer extends over said substrate second surface.
- 36. The structure of claim 33 further comprising a second substantially dopant-free, uninterrupted diffusion barrier layer over said substrate second surface.

37. The structure of claim 33, wherein said substantially dopant-free, uninterrupted diffusion barrier layer comprises one of the group consisting of silicon nitride and silicon oxynitride.

- 38. The structure of claim 33, wherein said at least one doped area comprises an impurity selected from the group consisting of an n-type impurity and a p-type impurity.
- 39. A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
  a semiconductor substrate having a first surface and a second surface;
  at least one first doped area on said substrate first surface;
  at least one second, differently doped area within said at least one first doped area; and a substantially dopant-free, uninterrupted diffusion barrier layer over said at least one first doped area on said substrate first surface.
- 40. The structure of claim 39 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.
  - 41. The structure of claim 39 wherein said substantially dopant-free, uninterrupted diffusion barrier layer extends over said substrate second surface.